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(71) Applicants and
(72) Inventors: **AYVAZYAN, Gagik** [AM/AM]; Avan, Varujan str. 10/19, 375101 Yerevan (AM). **SHABOYAN, Armen** [AM/AM]; Koreakan str. 14, 375082 Yerevan (AM).

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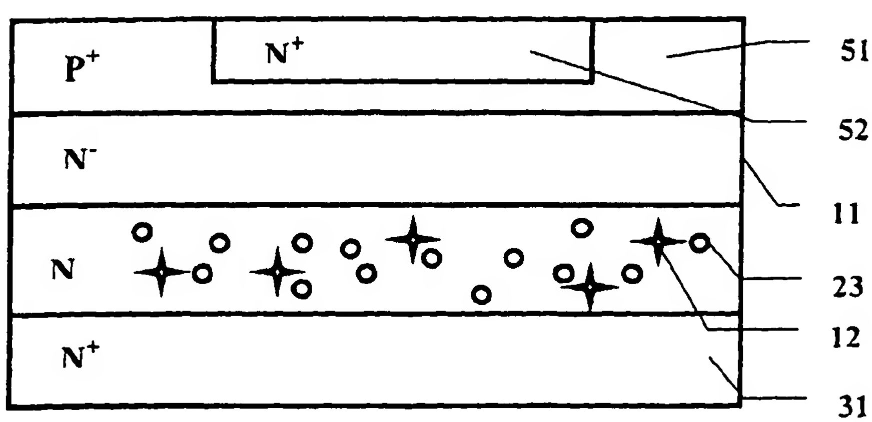
For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: METHOD OF MANUFACTURING POWER SILICON TRANSISTOR



(57) Abstract: The present invention relates to power semiconductor techniques and may be used for manufacturing of power silicon transistors. The method comprises steps providing the lightly doped N- silicon substrate, formation the porous silicon layer on the backside of substrate by anodic etching, and growing of the highly doped N+ epitaxial layer on the porous silicon layer.

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METHOD OF MANUFACTURING POWER SILICON TRANSISTOR

Technical Field

The present invention relates to power semiconductor techniques and may be used for manufacturing of power silicon transistors.

Background Art

In accordance with conventional prior art techniques power silicon transistors are manufactured on the base of silicon structure with $N - N^{+}$ collector junction, P^{+} base and N^{+} emitter regions. For providing optimal dynamic and static parameters of transistors, the forming of their base and emitter regions is realized by successive high temperature (1150 -1220^{0}C) diffusion of acceptor and donor impurity into a comparatively higher depth (respectively 10 -15 and 35-45 μm). Typical impurities employed are preferably aluminum, boron and gallium as acceptor one, and phosphorus - as donor one.

There is a method of manufacturing of power silicon transistor, which includes making of silicon $N - N^{+}$ structures by growing epitaxial layer on silicon substrate, forming P^{-} base and N^{+} emitter regions by successive diffusion of acceptor and donor impurity. This has been described in US Patent 5553566, 9/1996, Method of eliminating dislocations and lowering lattice strain for highly doped N^{+} substrates, H. Chiou et al.

According in this method N^{+} layer simultaneously is doped by the impurity with "compensating" atomic radius (for example, phosphorus and germanium). Germanium compensates for the atomic radius mismatch and also decreases of mechanical stress and dislocation on the interface of $N - N^{+}$ structures.

The disadvantage of this method is high density of diffusion-induced crystallographic defects into active regions of transistors. As a result electrophysical parameters of transistor structures is impaired. The other disadvantage of method is the low capability of transistors to second-breakdown, which is stipulated by an abrupt doping profile of $N - N^{+}$ collector junction, as it described in V. A. Belikov, V.A. Rudsky, and V.V. Togatov. Investigation of the impact of $N - N^{+}$ junction doping profile on capability of power transistors to second-breakdown // Electrotechnika, 7, 1991, p. 61 (in Russian). Provision of graded profile by creating of buffer epitaxial layer on the interface of $N - N^{+}$ collector junction, reduced the method productivity. This has been described in US Patent 5872028.

9/1996, Method of forming power semiconductor devices with controllable buffer. J.Yedinak et al.

One previously known method of manufacturing power silicon transistors was taught by A.A.Bogomyakow, J. V. Duchenko and V.A. Potapchuk, in SU Patent 1118237, which was issued on May 30, 1983 (in Russian). This method includes providing of the lightly doped N^- silicon substrate having a top and back surface, growing of the highly doped N^+ epitaxial layer on the backside of N^- silicon substrate, one-sided lapping and polishing of the substrate, forming P^+ base and N^+ emitter regions by successive diffusion acceptor and donor impurities from the top surface side of the substrate.

According to the present invention, after growing of N^+ epitaxial layer prolonged (10-14 hours) and high temperature (1200-1250°C) treatment of N - N^+ structures is carried out. It is supposed that there is an auto-doped of donor impurity from highly doped N^+ epitaxial layer to lightly doped N^- silicon substrate. As a result is provided graded doping profile of N - N^+ collector junction and therefore is increased the capability of transistors to second-breakdown.

The disadvantage of this method is availability of additional prolonged and high temperature treatment and high density of diffusion-induced defects (dislocations, dislocation networks, precipitates, dislocation half-loops, misfit dislocations etc.). As a result electrophysical parameters of transistor structures are impaired (for example, is decreased lifetime of minority charge carrier).

Disclosure of Invention

Therefore, the object of this invention is the improvement of electrophysical parameters of transistor structures and increase of the method productivity.

According to the present invention, as differentiated from the patent by A.A.Bogomyakow, et al., the porous silicon layer with the density of 1.4 + 1.6 g/sm^3 and depth of 10-15 μm is formed on the backside of N^- silicon substrate by anodic etching before growing of the epitaxial layer.

Invention is explained as follows. Porous silicon (PS) layers are anodicly produced on the silicon samples in an electrolyte containing hydrofluoric acid. Such technology is described in Y.S. Tsou, Y. Xiao, and C.A. Moore. Porous silicon. World Sci. Publ., NY, 1994, 412 p. The density and depth of PS layer is proportional to the concentration of the electrolyte, current density, anodic voltage and time.

The high diffusion rate of impurities in PS provided necessary graded doping profile of N - N^+ collector junction during comparative short time and low temperature treatment (for example, in process of forming P^+ base and N^+ emitter regions). Therefore, having the necessary density and depth of PS layer, the auto-doped of donor impurity from highly doped N^+ epitaxial layer to lightly doped N^- silicon substrate can be fully combined with the above-mentioned processing. In this case there is no need to carry out additional prolonged and high temperature treatment, that will result in the increase of the method productivity. It is significant that the formation process of PS does not requiring much time and energy expenditures.

Furthermore, during of thermo-diffusion treatment penetration and accumulation of initial and diffusion-induced defects take place in the PS layer (defects gettering), as it described in RU Patent 2120682, 4/1997, Method of producing silicon substrate, V. Skupov et al. (in Russian). As a result, the density of crystallographic defects in the active regions of transistors is decreasing that leads to the improvement of their electrophysical parameters.

The proposed meanings of density of PS layer $\rho = 1.4 \div 1.6$ g/sm^3 have the following grounds. The auto-doped rate of donor impurity and the efficiency of gettering sharply is decreased when $\rho > 1.6$ g/sm^3. Large mechanical stress can spring up in the PS layer in the case of $\rho < 1.4$ g/sm^3, which in turn are cause of generating additional crystallographic defects. This has been described in an article by Ayvazyan G.E. Anisotropic warpage of wafers with anodized porous silicon layers//Phys. Stat. Sol. (a), 175, N2, R7-R8, 1999.

The proposed meanings of PS layer depth h = 10-15 μm, are necessary and sufficient for providing the graded doping profile of N - N^+ collector junction in the process of forming base and emitter regions. This is described in V. A. Belikov, V.A. Rudsky. and V.V. Togatov. Investigation of the impact of N - N^+ junction doping profile on capability of power transistors to second-breakdown // Electrotechnika, 7, 1991, p. 61 (in Russian).

Brief Description of Drawings

The foregoing, and other objects, features and advantages of the invention will be apparent from the following, more particular description of the preferred embodiments. as illustrated in the accompanying drawing, wherein:

FIGS. 1-5 are schematic sectional view for explaining the steps of a method manufacturing of a power silicon transistor in accordance with our invention.

Best Mode for Carrying Out the Invention

Referring now to the drawing there is disclosed method manufacturing of a power silicon transistor in accordance with the teachings of the present invention. In FIG. 1 the substrate 11 of lightly doped N^--type silicon semiconductor material, typically 400 µm thick, having a resistivity 60 Om.cm and a number of defects 12 within crystalline lattice is provided. The substrate is provided with flat, smooth opposing top and back surfaces.

The manufacture of transistor structures on one group of substrates was carried out by a known method and on the other group by a present invention.

The manufacture of transistor structures by a present invention was carried out as follows. As shown in FIG. 2, the PS layer 21 was formed on the backside of N^- silicon substrate by anodic etching using an electrolyte containing hydrofluoric acid. Typically the substrate is first inserted within a suitable holding device and then immersed within the electrolyte. During immersion the substrate acts as an anode and a conductive member, which is likewise inserted within the electrolyte but is not readily dissoluble therein acts as a cathode. When anodic voltage is applied there between a reaction takes place causing gradual deep pore formation on the side wafer exposed to the electrolyte.

In the present example anodic etching was realized on the holding device for anodic treatment with the help of potentiostat. Solution of 48% hydrofluoric acid and ethyleneglycol in proportion 1:3 as an electrolyte was used. The amperemeter and voltmeter of the potentiostat ensured the regime of anodic etching, and consequently the required density and the depth of PS layer.

In the next operation, FIG. 3, the growth of high-doped N^+ layer 31 on the PS layer was implemented on the vertical reactor of epitaxial setup. The thickness of epitaxial layer was 180 µm, and a resistivity – 0.01 Om cm,

As shown in FIG. 4, the total thickness of substrate 41 was 300 µm after one-sided lapping and polishing of the substrate. Then follow conventional steps for forming an active device within the substrate 41.

In the next operation, FIG. 5, the P^+ base 51 was formed at temperature of 1220°C by successive diffusion of gallium and boron, and N^+ emitter 52 - by diffusion of phosphorus at the temperature of 1150°C. The final depth of base region was 43.0 ± 3.0 µm, and 15.0 ± 0.5 µm for emitter region. There was a simultaneous the auto-doped of donor impurity from highly doped N^+ epitaxial layer to lightly doped N^- silicon substrate and gettering of initial and diffusion-induced defects in N PS layer.

In subsequent operations (not shown), contacts are made to the emitter, base and collector regions. Typically, contacts to the emitter and base regions are made from the top surface and to the collector region from the back surface.

The lifetime of minority charge carriers was controlled in the manufacturing process of power transistor structures and the assessments of operating parameters of finished transistors was carried out. The lifetime of minority charge carriers was less than 10 μs in case $\rho < 1.4$ g/sm^3 and $\rho > 1.6$ g/sm^3, and 15-45 μs in case $\rho = 1.4 \div 1.6$ g/cm^3. The lifetime of minority charge carriers was independent from the depth of PS layer.

The maximum second-breakdown voltage of transistor was observed in depth h = 10-15 μm of the PS layer. The decreasing of depth led to the voltage reduction. The second-breakdown voltage remained unchanged at h >15 μm.

The assessments of operating parameters of transistors, manufactured in different ways evidenced that the proposed method enables to increase voltage of collector emitter and second-breakdown voltage of devices 1.2-1.3 times. Furthermore. productivity will be increased, since prolonged and high temperature treatment are replaced with the formation of PS layer not requiring much time and energy expenditures.

Thus far a specific method for manufacturing of a power silicon transistor using an N – N$^+$ structure has been described. It will be appreciated, however, that the teachings of the present invention may be put to use when making other type devices. Numerous changes can be made without parting from the spirit and scope of the invention.

CLAIMS

A method of manufacturing of power silicon transistors comprises the steps of:

- providing a lightly doped N^- silicon substrate having a top and back surface;
- forming a porous silicon layer with the density of 1.4 + 1.6 g/sm^3 and depth of 10-15μm on the backside of N^- silicon substrate by anodic etching;
- growing of a highly doped N^+ epitaxial layer on the porous silicon layer;
- one-sided lapping and polishing of substrate;
- forming a P^+ base and N^+ emitter regions by successive diffusion of acceptor and donor impurities from the top surface side of substrate.

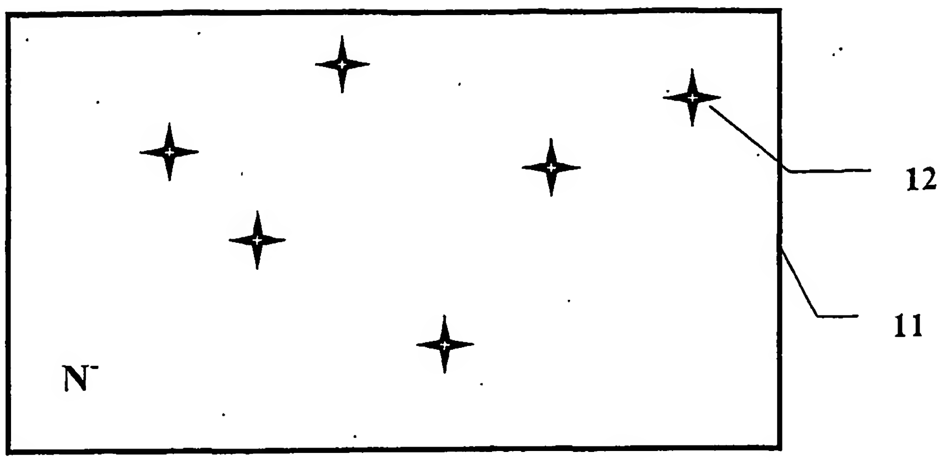

FIG. 1.

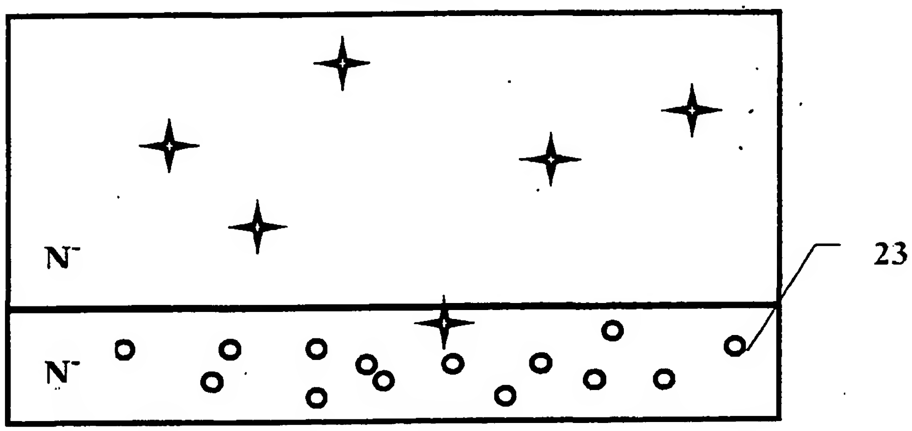

FIG. 2.

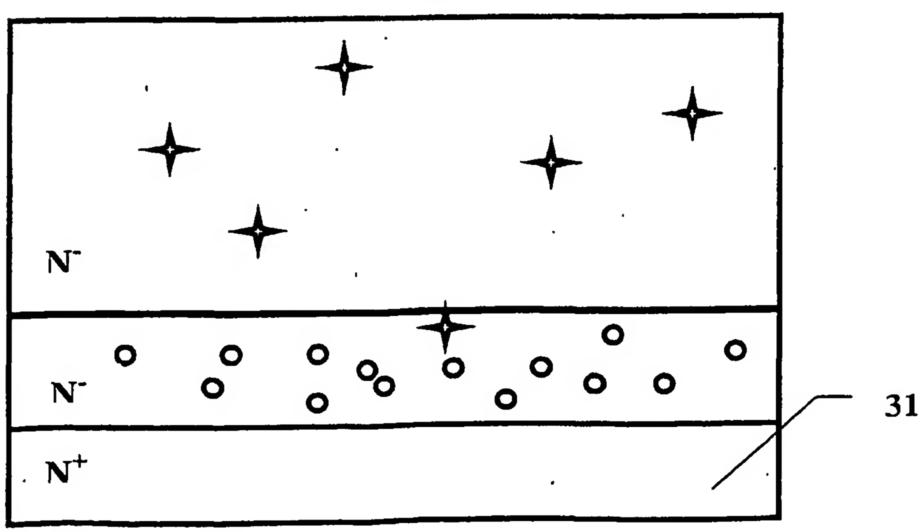

FIG. 3.

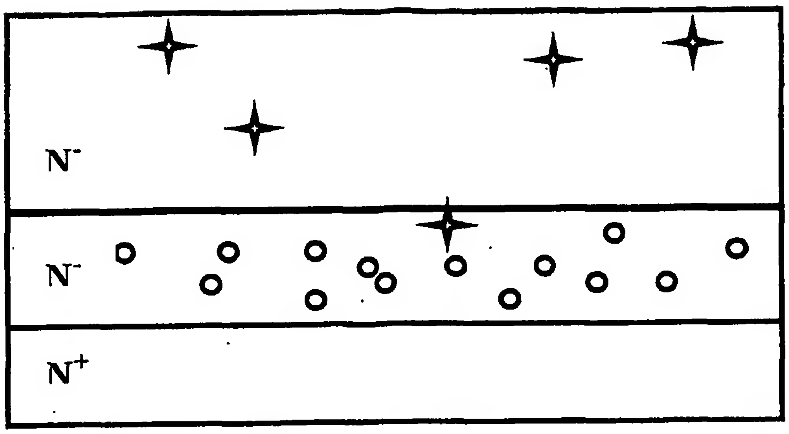

FIG. 4.

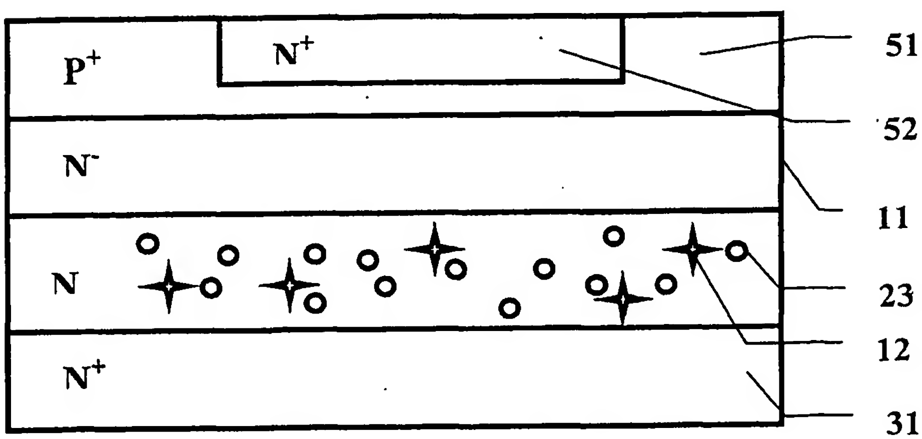

FIG. 5.

INTERNATIONAL SEARCH REPORT

International application No.
PCT/AM 01/00002

A. CLASSIFICATION OF SUBJECT MATTER

H01L 21/331, 21/322

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L 21/322, 21/331

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched:

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No
A	Зарубежная электронная техника. ЦНИИ "Электроника", 1978, август, № 15, страницы 42-45	1
A	SU 1827143 A3 (ТОВАРИЩЕСТВО С ОГРАНИЧЕННОЙ ОТВЕТСТВЕННОСТЬЮ "КМК") 27.06.1996	1
A	US 3929529 A (INTERNATIONAL BUSINESS MACHINES CORPORATION) Dec. 30, 1975	1
A	Зарубежная электронная техника. Москва, 1983, 11(270), страницы 33-36	1
A	SU 240852 A (Ф.П. ПРЕСС и др.) 25.VIII.1969	1

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Name and mailing address of the ISA/RU FIPS	Authorized officer
Russia, 121858, Moskva, Berezhkovskaya nab., 30-1	N. Listvina
Facsimile No.	Telephone No. (095)240-25-91